	L #	Hits	Search Text	DBs	Time Stamp
1	L1	398232	fuji.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 15:17
2	L2	43539	"gate insulating"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 15:17
3	L3	491	L1 and L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 15:17
4	L4	413	L3 and ((@ad<"20010530") or (@rlad<"20010530"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:42

	L #	Hits	Search Text	DBs	Time Stamp
5	L5	60	4 and drift	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 15:25
6	L13	10	(("5122848") or ("6316807") or ("6624470") or ("6639274") or ("6664163")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:25
7	L14	19	("4116720" | "4199774" | "4272302" | "4359816" | "4364073" | "4364074" | "4374455" | "4464212" | "4476622" | "4503598" | "4543706" | "4566172" | "4567641" | "4650544" | "4758528" | "4859622" | "4890144" | "4920065" | "4941026").PN.	US-PGPUB; USPAT; USOCR	2005/06/19 15:43
8	L15	72	("5122848").URPN.	USPAT	2005/06/19 15:44
9	L16	70	15 and ((@ad<"20010530") or (@rlad<"20010530"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 15:45

	L #	Hits	Search Text	DBs	Time Stamp
10	L17	47	16 and "drain region"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:25
11	L18	0	17 and "second conductor"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:25
12	L19	26	17 and base	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:26
13	L20	24	19 and bottom	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:26

	L #	Hits	Search Text	DBs	Time Stamp
14	L21	1	20 and uniform	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:42
15	L22	4330	Fujishima.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:42
16	L23	3563	22 and ((@ad<"20010530") or (@rlad<"20010530"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:42
17	L24	29	23 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/19 16:43

US-PAT-NO: **6664163**

DOCUMENT-IDENTIFIER: US 6664163 B2

TITLE: Low on-resistance **trench** lateral MISFET with better switching characteristics and method for manufacturing same

---------- KWIC ---------

Abstract Text - ABTX (1):

A high-voltage and low on-resistance semiconductor device incorporates a **trench** structure that provides improved switching characteristics. In a preferred embodiment, a **Trench** Lateral Power MISFET is provided having a gate, channel and **drift regions** that are built on the side-walls of the **trench**. The process used to form the MISFET involves a self-aligned **trench** bottom contact hole to contact a source provided at the bottom of the **trench** to achieve minimum pitch and very low on-resistance. An example of a MISFET with 80 V breakdown voltage having a cell pitch of 3.4 microns is disclosed in which an on-resistance of 0.7 m.OMEGA.-cm.sup.2 is realized. The switching characteristics of the MISFET are twice as good as that of prior MISFET device structures.

US Patent No. - PN (1):

6664163

TITLE - TI (1):

Low on-resistance **trench** lateral MISFET with better switching characteristics and method for manufacturing same

Brief Summary Text - BSTX (2):

The invention relates in general to lateral semiconductor devices including a **trench** structure, and a method of manufacturing such devices. More specifically, the invention relates to MISFETs with a high breakdown voltage and a low on-resistance, which can be incorporated in integrated

circuits,
power supplies, motors and other devices.

Brief Summary Text - BSTX (4):

An example of one type of conventional high voltage lateral MISFETs with low on-resistance characteristics is shown in FIG. 1. A high resistive n.sup.- extended drain 10 is formed in a p.sup.- substrate 8 between a p base region 12 and an n.sup.+ **drain region** 14 to reduce an electric field between a source region 16 and the **drain region** 14. A gate oxide layer 18 under a **gate electrode** 20 is thicker at the drain side in order to reduce electric field in the n.sup.- extended drain 10. Generally, lateral MISFETs consist of the following four regions shown in FIG. 1: (1) a source region with a distance of l.sub.1, (2) a channel region with a distance of l.sub.2, (3) an extended **drain region** with a distance of l.sub.3, and (4) a **drain region** with a distance of l.sub.4. The pitch of the device is the sum of l.sub.1 +l.sub.2,+l.sub.3 +l.sub.4 and determines the packing density of the device and its specific on-resistance. The smaller the pitch, the higher the packing density and the lower the on-resistance per unit area. Present state of the art MISFETs with a breakdown voltage of 80 V require l.sub.3 to be 3 .mu.m to reduce the electric field near the drain and prevent premature breakdown. The remaining parameters (l.sub.1, l.sub.2, and l.sub.4) do not influence the breakdown voltage significantly and are required to be 1.5 .mu.m, 2 .mu.m, and 1.5 .mu.m respectively for l.sub.1, l.sub.2 and l.sub.4 (for a 1 .mu.m design rule). Thus, the distance or length of the n.sup.- extended drain 10 is the largest among all of the regions and must be increased as the breakdown voltage of the MISFET increases. As a result, the packing density of the MISFET is sacrificed and on-resistance increases. MISFETS with the above-described structure have

already been described. See, for example, T. Efland, et al., "Self-Aligned
RESURF To LOCOS Region LDMOS Characterization shows Excellent Rsp vs BV
Performance" Proceedings ISPSD'96, pp. 147-150, 1996, the contents of which
are incorporated herein by reference.

Brief Summary Text - BSTX (6):

To overcome the packing density limitation discussed above, MISFETs using
trench structures have been proposed by N. Fujishima, et al. in U.S. patent
application Ser. No. 08/547,910. As illustrated in FIG. 3, a channel 24 and
an n.sup.- extended drain 26 are located vertically at a side-wall of a **trench**
formed in a substrate 28. Since the **trench** MISFET has the n.sup.- extended
drain 26 between a source region 31 and a **drain region** 32, and a thick gate
oxide 34 between a **gate electrode** 36 and the **drain region** 32, it is possible to
optimize the structure to get almost the same current handling capability in
the unit cell as the conventional MISFET without reducing the breakdown
voltage. The pitch in this case is determined by the sum of 1.sub.1, 1.sub.6,
and 1.sub.5, which typically have values of 1.5 .mu.m, 2.0 .mu.m and 0.5 .mu.m
respectively (for minimum 1 .mu.m design rules) resulting in half the pitch of
the structure in FIG. 1. Therefore, packing density per unit area of the
MISFET can be increased and a reduction in on-resistance per unit area
achieved.

Brief Summary Text - BSTX (7):

However, for the device of FIG. 3, two additional masks are needed to define
the silicon **trench** and the drain contact holes. The resulting process also
requires strict alignment tolerance among these three masks. In addition, two
deep directional etching steps are needed to define the gate and make the drain
contact hole inside the initial silicon **trench**.

the
bottom of a **trench** 204 and an extended drain 206 is located at the upper
portion of the **trench** sidewall. One of the advantages of this structure is
that Cgd (Miller capacitance) would be reduced to less than half of that of the
first embodiment because the plugged polysilicon 208 at the bottom of the
trench 204 contacts the source 202 instead of the drain 206. Thus Cgd is
generated only between the gate 210 and n.sup.- drain 206.

Detailed Description Text - DETX (12):
The process to manufacture the second embodiment will utilize a self-aligned
method to form the **gate electrodes and the trench** bottom contact holes to the
source to achieve minimum pitch and very low on-resistance. The source contact
holes will be filled with polysilicon to access the bottom source from the
surface and to level the surface for metal formation.

Detailed Description Text - DETX (14):
As shown in FIG. 27, the MISFET is formed along the sidewalls of the
trenches. The drain contact 212 is located at the surface. The channel,
n.sup.- drain 206, gate oxide 214, thick oxide 216, and **gate electrode** 210 are
formed along the sidewalls. The n.sup.+ source 202 at the bottom of the **trench**
204 is connected and brought to the surface through a polysilicon plug 208.
When a positive bias, higher than the threshold voltage, is applied to the gate
210, an inversion layer is created and an electron current flows from the
source electrode 218 through the polysilicon plug 208 to the n.sup.+ source 202
at the bottom of the **trench** 204, and is collected by the drain 220 at the
surface. In order to decrease the electric field under the gate 210, a thick
oxide 216 is used at the top of the sidewall. The (100) sidewall plane, which
has been shown to have the lowest interface-trap density and the highest
surface electron mobility, is used in the implementation of the

device by
orienting the main sidewall plane 45.degree. away from the
<110> axis of
the (100) orientation wafer. In addition, the current in the n.sup.-
drain 206
flows mainly in the bulk instead of at the surface, thus avoiding
mobility
degradation due to damage associated with **trench** formation.

Detailed Description Text - DETX (15):
Brief explanation of device dimensions are described in FIG. 28.
The depth
of the second **trench** 1.sub.14 is about 2 .mu.m. Total depth of the
trench
1.sub.15 is about 5 .mu.m. The length of the source contact 1.sub.11
the
distance between the source and drain 1.sub.12, and the length of the
drain
1.sub.13 are 0.5, 2.0, and 1.5 .mu.m, respectively under 1 .mu.m
design rule.
Usage of 0.6 .mu.m minimum feature size reduces 1.sub.11 and 1.sub.13
to 0.3
and 0.9 .mu.m, respectively.

Detailed Description Text - DETX (16):
The process used in the fabrication of the second embodiment is
illustrated
in FIGS. 29 to 36. First, n.sup.- diffusion is performed using the
first mask.
The obtained junction depth and surface concentration of the
diffusion are
about 1 .mu.m and 1e17-cm.sup.-3, respectively. Then a shallow
trench whose
depth is 3 .mu.m is etched in a p-type silicon substrate using the
second mask.
Thereafter the p body and n.sup.- drain are formed by using tilted
ion-implantation (FIG. 29). After the p body and n.sup.- drain are
driven, wet
oxidation is performed to grow a thick oxide at the bottom of the
trench as
well as at the surface. The junction depth of the n.sup.- drain is
about 1
.mu.m. The surface concentration of the n.sup.- drain is about 1e17-
cm.sup.-3.
The thickness of the grown oxide is about 0.5 .mu.m (FIG. 30). Next,
the oxide
and the second silicon **trench** is etched using RIE. The additional
etching
depth 1.sub.14 is 2 .mu.m. Since RIE etching is anisotropic, most of
the oxide

remains on the sidewall (FIG. 31). After the 0.1 .mu.m gate oxide is formed,
polysilicon with a thickness of 0.5 .mu.m is deposited (FIG. 32). A further
oxide layer is deposited on the surface. The oxide layer at the top is
selectively etched using the third mask to define the actual gate area. The
polysilicon is etched by RIE using the top oxide layer as a mask. Then the p
base and n.sup.+ region are formed using 4th and 5th masks. The junction
depths of the p base and n.sup.+ region are 1.0 and 0.2 .mu.m, respectively.
The surface concentration of the n.sup.+ is 1e20-cm.sup.-3 (FIGS. 33 (a) and
(b)).

Detailed Description Text - DETX (17):

A critical part of the process is the creation of contact holes at the
bottom of the **trench**. A 1.0 .mu.m oxide layer is deposited by CVD in the
trench as illustrated in FIG. 34 (a) and (b). Because the reactants do not
migrate rapidly along the surface at the temperature of about 400.degree. C.
used for CVD, the oxide inside the **trench** is thinner than that at the surface
(t.sub.2 <t.sub.1) [5]. RIE is then used to remove the oxide by 0.5 .mu.m
directionally. This creates a contact hole at the bottom of the **trench** as
shown in FIG. 35(a). Since RIE has strong directional etching properties, the
oxide film at the bottom of the **trench** is completely removed and the silicon is
exposed. On the other hand, the oxide at the sidewalls and at the top surface
is retained and is thick enough to provide good electrical isolation between
the gate and the source.

Detailed Description Text - DETX (19):

FIG. 38 lists a comparison of switching figure of merit between the first
embodiment and second embodiment **trench** lateral MISFETs. Since the Cgd for the
second embodiment MISFET is half of the first embodiment MISFET, the figure of

merit for the second embodiment MISFET is twice as good as the conventional
one.

Detailed Description Text - DETX (20):
Trade off between specific on-resistance and breakdown voltage is shown in
FIG. 37. On-resistance of the proposed **trench** lateral MISFET will be reduced
by about 50% (using a 0.6 .mu.m minimum feature size), bringing it close to the
silicon limit (0.7 m.OMEGA.-cm.sup.2 for an 80 V device).

Detailed Description Text - DETX (21):
The invention has been described with reference to certain preferred
embodiments thereof. It will be understood, however, that modifications and
variations are possible within the scope of the appended claims. The method of
forming the thick oxide inside the **trench** and creating contact holes at the
trench bottom is useful not only for MISFETs, but can be employed to
manufacture other devices including diodes, bipolar transistors, IGBTs and
MESFETs and DRAM cells which require a contact at the bottom of a **trench**.

Claims Text - CLTX (1):
1. A method of manufacturing a MISFET comprising the steps of: a) forming a
trench in a substrate of first conductive type; b) forming a first region of
the first conductivity type and a second region of the second conductivity type
into the substrate through portions of the **trench**; c) depositing an oxide
layer on portions of sidewalls of the **trench**, wherein said oxide layer extends
from the top of the **trench**; d) then forming an extended **trench** while retaining
said oxide layer on the portions of the sidewalls of said **trench**; e) forming a
gate oxide layer on the sidewalls of said extended **trench**; f) forming a gate
layer on the gate oxide layer;

Claims Text - CLTX (2):
selectively etching the gate layer, and the gate oxide layer so that the

surface of the substrate is exposed in regions adjacent to the **trench** and residual films of the gate layer and the gate oxide layer are left on the sidewalls of the **trench**; g) forming a base of the first conductivity type and a source of the second conductivity type at the bottom of the **trench**; h) forming a second oxide layer inside the **trench** and on the surface of the substrate over a drain by a method where oxide growth rate is slower inside the **trench** than at the surface of the substrate, wherein the thickness of the second oxide layer within the **trench** is less than the thickness of the second oxide layer on the surface of the substrate; i) etching the oxide layer at the bottom of the **trench** to form a contact hole that extends to the substrate while maintaining a thickness of the second oxide layer on the sidewalls of the **trench** and surface of the substrate using a directional etching method; and j) forming an electrical interconnection material in the **trench** that extends through the contact hole.

Claims Text - CLTX (3):

2. A method of manufacturing an MISFET comprising: a) selectively forming a second conductivity type diffusion layer in a surface region of a first conductivity type silicon substrate; b) forming a first **trench** in the silicon substrate; c) forming a first conductivity body and a second conductivity **drain region** in the silicon substrate by implantation through side walls of the first **trench**; d) forming a thick oxide layer in the first **trench** and on the surface of the silicon substrate; e) then etching through the thick oxide layer and into the silicon substrate to form a second **trench**; d) forming a gate oxide layer in the second **trench**; e) depositing a polysilicon layer over the gate oxide layer and the thick oxide layer; f) forming a top oxide layer and selectively etching the top oxide layer to define a gate area;

g) etching the polysilicon layer using the top oxide layer as a mask; h) forming a first conductivity type base region in the silicon substrate under the bottom of the second **trench**; i) depositing an oxide layer in the second **trench**, wherein the oxide inside the second **trench** is thinner than that at the surface of the silicon substrate; j) forming a contact hole at the bottom of the second **trench**; k) filling the contact hole with polysilicon; and l) opening contact windows in the polysilicon and filling the contact holes with metal.

Related Application Filing Date - RLFD (1):
19981231

Related Application Filing Date - RLFD (2):
19971205

Other Reference Publication - OREF (3):
"A New Vertical Power **MOSFET** Structure with Extremely Reduced On-Resistance"; Ueda et al.; IEEE Transactions on Electron Devices; vol. ED-32, No. 1; Jan. 1983; pp. 2-6.

Other Reference Publication - OREF (4):
"A **trench** lateral power **MOSFET** using self-aligned **trench** bottom contact holes"; Fujishima et al.; International Electron Devices Meeting; Dec. 7-10, 1997; Washington D.C.; 4 pgs.